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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,472	09/10/2003	Nadi R. Itani	0876-CS-D1	4320

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EXAMINER	
LAM, HUNG H	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,472	ITANI ET AL.	
	Examiner	Art Unit	
	HUNG H. LAM	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/17/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-14 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-14 and 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 11/15/07 and 12/17/07, have been entered and made of record. Claim 38 is added. Claims 1-2 and 15-34 are canceled. Claims 2-14 and 35-38 are pending.

In review of Applicant's amendment claim 10, the objection of claim 10 is hereby withdrawn.

Response to Arguments

2. Applicant's arguments see Amendment (Remarks), pages 5-7, filed 11/15/07, with respect to the rejection(s) of claim(s) 2-14 and 35-38 have been fully considered but they are not persuasive.

The Applicants argue that the Simerly reference and/or the DeAngelis reference, either taken alone or in combination thereof, do not in any way teach or suggest an automatic gain control circuit (AGC) receiving the determined gain or determined gain values and the AGC having a gain splitter circuit that produces from or splits the determined gain or determined gain values into distributed gain values. The Examiner respectfully disagrees. Simerly teaches an AGC (32 and/or ASIC 40) receiving digital control signal (C2) generated by ASIC 40 (see Fig. 2; Col. 3, Ln. 49-67; Col. 4, Ln. 29-31). Signals outputted from AGC 32 are then fed to summation 34, ADC 36 and to ASIC

40 (see Fig. 2). The ASIC 40 is further interpreted as the splitter because after receiving signals outputted from AGC 32, the ASIC 40 also generates digital control signal C6 which possibly controls the aperture iris (Col. 3, Ln. 49-67; Col. 4, Ln. 35-38; Col. 5, Ln. 10-13) and raises or lowers the maximum amplitude of a video signal without (Col. 4, Ln. 20-27).

The Applicants further argue that the cited prior references, either taken alone or in combination thereof, do not in any way teach or suggest that the distributed gain values include at least the shutter gain, the analog gain, and the digital gain. The Examiner respectfully disagrees. Simerly teaches that the control signal C6 which is possibly used for controlling aperture iris (Col. 4, Ln. 35-38; Col. 5, Ln. 10-13). Since the output signal levels of AGC 32 and summation 34 can be controlled by ASIC 40 (Col. 3, Ln. 49-Col. 4, Ln. 45), the analog gain is interpreted as S6 and S8 (see Fig. 2) wherein digital gain is interpreted as digital signals 510, C2 and C6 (see Fig. 2).

In view of the above, the Examiner believes that the broadest interpretation of the present claimed invention does in fact read on the cited reference for at least the reasons discussed above and as stated in the detail Office Action as follows. This Office action is now made final.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 3-12, 14 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Simerly (US-5,982,424).

With regarding **claim 3**, Simerly discloses a distributed gain control circuit (DGCC) comprising:

an imager signal source including a shutter (Fig. 1; iris 12; Col. 3, Ln. 16-22; Col. 5, Ln. 9-15);

a timing circuit for controlling said shutter and the production of signals from said imager signal source (Fig. 2; clock drivers);

a CDSNGA system (Fig. 2; CDS 30) for receiving imager signals from said imager signal source (CCD card 20);

an analog to digital converter (A/D 36) connected to said CDSNGA system for receiving an amplified imager signal stream from said CDSNGA system and converting the amplified imager signal stream into digital form (see the connection between A/D 36 and CDS 30);

a digital gain circuit connected to said analog to digital converter (see AGC 32); and

an automatic gain control circuit (ASIC 40 and/or AGC 32) having a gain splitter circuit (ASIC 40) for receiving gain values which the digital gain circuit have determined and wherein the gain splitter circuit produce distributed gain values from the received gain values (see Fig. 2; Col. 3, Ln. 49-67; Col. 4, Ln. 29-31: Simerly teaches an AGC 32 and/or ASIC 40 receiving digital control signal C2 generated by ASIC 40. Signals outputted from AGC 32 are then feed to summation 34, ADC 36 and to ASIC 40. Col. 3, Ln. 49-67; Col. 4, Ln. 20-38; Col. 5, Ln. 10-13: The ASIC 40 is further interpreted as the splitter because after receiving signals outputted from AGC 32, the ASIC 40 also generates digital control signal C6 which possibly controls the aperture iris and raises or lowers the maximum amplitude of the video signal).

With regarding **claim 4**, Simerly discloses the DGCC according wherein said AGC circuit is coupled to said timing circuit for controlling the production of signals from said imager signal source (Fig. 2; see the connection from ASIC 40 to clock drivers).

With regarding **claim 5**, Simerly discloses a method of gain control in an imaging system having a shutter (12), a digital gain circuit (AGC 32), and a CDSNGA circuit (CDS 30), including:

determining total gain for an imaging system (Col. 3, Ln. 22-Col. 4, Ln. 20);

receiving, by an automatic, gain control (AGC) circuit having a gain splitter circuit, the determined total gain (see Fig 2; Col. 3, Ln. 49-67; Col. 4, Ln. 20-38; Col. 5, Ln. 10-

13: The ASIC 40 is further interpreted as the splitter because after receiving signals outputted from AGC 32, the ASIC 40 generates control signals C2, C6, C62 and C64);

splitting, by the gain splitter, circuit, the determined total gain into distributed gain values which at least include a shutter gain (Col. 4, Ln. 35-38; Col. 5, Ln. 10-13), an analog gain (VGA: Fig. 2; see S6 and S8), and a digital gain (Fig. 2; see 510, C2 and C6); and

determining the level of the shutter gain to be applied in the operation of the imaging system (Col. 5, Ln. 9-20; shutter gain is inherently determined in order to control the amount of aperture opening of lens 8);

determining the level of the analog gain to be applied in the operation of the imaging system (see AGC 32; Col. 3, Ln. 22-Col. 4, Ln. 20; the claim is broadly written; therefore, the Examiner broadly interpreted the AGC 32 or a CCD amplifier which inherently includes in a CCD as analog gain to be applied in the operation of the imaging system); and

determining the level of the digital gain to be applied in the operation of the imaging system (Fig. 2; see connection from AGC 32 to ADC 36 and digital signal 510; the gain of the digital signal 510 from A/DC 36 is inherently determined in accordance with the analog gain generated by AGC 32).

With regarding **claim 6**, Simerly discloses the method wherein each gain setting for said imaging system is applied for the duration of a single frame (abstract; Col. 2, Ln. 10, 35; Col. 7, Ln. 20-Col. 9, Ln. 9).

With regarding **claim 7**, Simerly discloses the method including hierarchically adjusting the shutter gain (Col. 4, Ln. 35-38; Col. 5, Ln. 10-13), the analog (VGA) gain (S6-S8), and the digital gain (see Fig. 2; digital signal 510 is inherently adjusted accordance with the analog gain AGC 32).

With regarding **claim 8**, Simerly discloses the method wherein the shutter gain has maximum and minimum shutter gain values (Col. 3, Ln. 16-22; Col. 5, Ln. 9-15: a maximum and minimum shutter gain values are inherently included in order to open or close the iris 12).

With regarding **claim 9**, Simerly discloses the method wherein the analog (VGA) gain has maximum and minimum analog gain values (AGC 32; Col. 3, Ln. 22-Col. 4, Ln. 20).

With regarding **claim 10**, Simerly discloses the method wherein a chip gain has a maximum and a minimum gain value (AGC 32; Col. 3, Ln. 22-Col. 4, Ln. 20).

With regarding **claim 11**, Simerly discloses the method wherein the digital gain has a maximum and a minimum value (see connection from AGC 32 to A/D 36 and digital signal 510; Col. 3, Ln. 22-Col. 4, Ln. 20).

With regarding **claim 12**, Simerly discloses the method wherein the analog (VGA) gain and the digital gain remain at a constant level as the shutter gain is varied (Fig. 2; The analog gain and the gain of digital signal 510 are inherently varied or fixed accordance to one another. It is noticed that the Iris control signal line C62 is differed from AGC control signal line C2. Therefore, it is inherent that the analog and the digital gain remain at a constant level while the shutter gain can be varied).

With regarding **claim 14**, Simerly discloses the method wherein the shutter gain and the digital gain remain at a constant level as the analog (VGA) gain is varied (it is inherent that the AGC 32 is controlled and operated differently from an inherent CCD amplifier; therefore, the shutter gain and the digital gain can be remained at a constant level while the CCD amplifier is inherently varied).

With regarding **claim 38**, Simerly the DGCC according to claim 3 wherein the distributed gain values are split into shutter gain values (Col. 4, Ln. 35-38; Col. 5, Ln. 10-13), analog gain values (Fig. 2; see S6, S8, C62 and C64), and digital gain values (Fig. 2; see 510, C2 and C6).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 13 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simerly in view of DeAngelis (US-5,657,077).

With regarding **claim 13**, Simerly discloses the wherein the shutter gain and the analog (VGA) gain remain at a constant level (it is inherent that both shutter gain and analog gain remain at constant). However, Simerly fails to explicitly disclose that the shutter gain and the analog (VGA) gain remain at a constant level as the digital gain is varied.

In the same field of endeavor, DeAngelis teaches a camera system also include a grey scale gain controller to adjust the digital output signal according to a pre-selected gain level, preferably selectable at the main control computer and preferably to a gain level corresponding to the digital values in the captured frames (Col. 3, Ln. 10-23). DeAngelis further teaches that the camera is completely computer controlled from a remote location for controlling focus, zoom, pan and all other camera functions (Col. 3, Ln. 19-23). In light of the teaching from DeAngelis, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Simerly by allowing a computer control to remotely control all other camera functions. The modifications thus allow the camera to be manipulated by a remote computer.

With regarding **claim 35**, Simerly fails to explicitly disclose the method wherein said constant level is user-settable.

In the same field of endeavor, DeAngelis teaches a camera wherein a user can select how fast the AGC control of the camera operates by adjusting the bandwidth of the gain control and thereby appropriately improving the displayed screen contrast (Col. 9, Ln. 20-44). In light of the teaching from DeAngelis, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Simerly by allowing a user to adjusting the bandwidth of the gain control. The modifications thus appropriately improve the displayed screen contrast (DeAngelis: Col. 9, Ln. 20-44).

With regarding **claim 36**, the claim contains the same limitations as claimed in claim 35. Therefore, claim 36 is analyzed and rejected as previously discussed in claim 35.

With regarding **claim 37**, the claim contains the same limitations as claimed in claim 35. Therefore, claim 37 is analyzed and rejected as previously discussed in claim 35.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUNG H. LAM whose telephone number is (571)272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, LIN YE can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

03/14/08

/Lin Ye/
Supervisory Patent Examiner, Art Unit 2622